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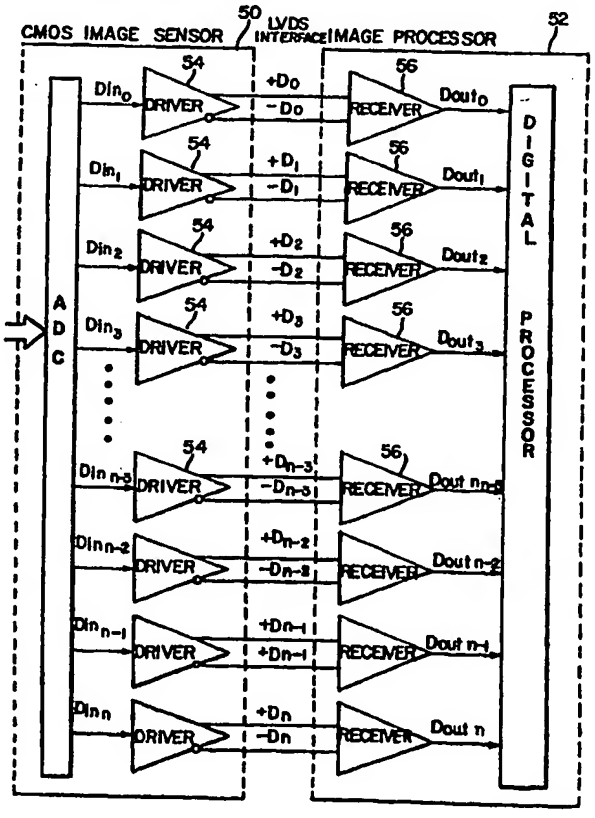
(54) Title: LOW COST LINE–BASED VIDEO COMPRESSION OF DIGITAL VIDEO STREAM DATA

(57) Abstract

CMOS imaging apparatus including first and second chips, the first chip having formed thereon a CMOS image sensor, an analog to digital converter circuit, and a CMOS driver circuit providing first and second differential outputs. The second chip includes a CMOS digital signal processor and a plurality of CMOS receiver circuits, each having a pair of differential inputs adapted to be connected to the plurality of differential outputs of the first chip to form a series of low voltage differential signaling circuits. Implementation of the invention facilitates implementation of CMOS image sensors containing at least one million light responsive pixel image sensors wherein data is transferred between the CMOS image sensor and the CMOS image processor at data rates of 30 MHz or more.



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LOW COST LINE-BASED VIDEO COMPRESSION OF DIGITAL VIDEO STREAM DATA

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to image processing and more specifically pertains to a video compression algorithm for increasing the data throughput on a limited bandwidth link between a host and a digital video camera.

2. Description of Related Art

A digital image represents a two-dimensional array of samples, where each sample is called a pixel. Precision determines how many levels of intensity can be represented and is expressed as the number of bits/sample. Resolution of an image refers to its capability to reproduce fine details. Higher resolution requires more complex imaging systems to represent these images in real-time. In video systems, resolution refers to the number of line pairs resolved on the face of the display screen, expressed in cycles per picture height, or cycles per picture width. Full motion video is characterized with at least a 24-Hz frames/sec, and 30 or even 60 frames/sec for high definition TV. For animation, acceptable frame rate is in the range 15-19 frames/sec while for video telephony it is 5-10 frames/sec. Videoconferencing and interactive multimedia applications require the rate of 15-30 frames/sec.

Commercial imaging applications are surfacing in digital broadcast television, compact disk video, multimedia, video teleconferencing systems, dynamic medical imaging devices, and high definition TV. Imaging applications are time critical and computationally and data intensive, and require both the storage and transmission of enormous data sets which can be accomplished with image compression. Achieving the compression ratios necessary for digital video involves the processing of individual images to remove spatial redundancies and a motion analysis of the sequence to remove temporal redundancies.

square of the charging voltage, i.e., the voltage level of the ADC's digital output signal. The conventional single ended signaling method uses charging voltages between 2.7 and 5 volts, which entails increasingly undesirable power consumption as frequencies increase. Thus, creation of higher resolution CMOS video images has faced significant obstacles.

OBJECTS AND SUMMARY OF THE INVENTION

It is therefore an object of the invention to improve CMOS imaging systems;

It is another object of the invention to reduce power consumption of such systems;

It is another object of the invention to provide improved apparatus for transmitting the output of a CMOS image sensor to a digital signal processor;

It is still another object of the invention to provide for faster, more efficient pixel data transmission in CMOS imaging apparatus;

It is yet another object of the invention to facilitate production of CMOS imaging apparatus of greatly improved resolution.

These and other objects and advantages are achieved according to the invention by provision of CMOS imaging apparatus comprising a CMOS image sensor, a CMOS image processor, and a plurality of low voltage differential signaling circuits connected between the image sensor and the image processor. Each low voltage differential circuit comprises a CMOS driver circuit, a CMOS receiver circuit, and a pair of transmission lines interconnecting the driver circuit and receiver circuit. Each low voltage differential signaling circuit transfers a portion of the output of the image sensor

array to a receiver communicating with the digital signal processor. In this manner, extremely low power and low noise high speed operation is achieved.

According to one illustrative embodiment, the CMOS imaging apparatus comprises first and second silicon substrate chips. The first chip has formed thereon a CMOS image sensor including an analog to digital converter circuit, which provides a plurality of digital pixel signal value output signals. The first chip further includes a plurality of CMOS driver circuits, each receiving as an input a selected one of the plurality of digital pixel signal value output signals and having first and second differential outputs. The second chip includes a CMOS digital signal processor formed thereon which has a plurality of inputs connected to respective outputs of a plurality of CMOS receiver circuits. Each CMOS receiver circuit has a pair of differential inputs adapted to be connected to the differential outputs of the first chip. The apparatus further includes a pair of transmission lines connected between each respective pair of differential outputs and differential inputs.

Implementation of the invention permits use of a CMOS image sensor containing at least one million light responsive CMOS pixel image sensors wherein data is transferred between the CMOS image sensor and the CMOS image processor at a data rate of 30 MHz or more.

BRIEF DESCRIPTION OF THE DRAWINGS

The objects and features of the present invention, which are believed to be novel, are set forth with particularity in the appended claims. The present invention, both as to its organization and manner of operation, together with further objects and

advantages, may best be understood by reference to the following description, taken in connection with the accompanying drawings, of which:

Figure 1 is a circuit schematic of a low voltage differential signaling circuit; and

Figure 2 is a circuit diagram of the preferred embodiment of the invention.

DETAILED DESCRIPTION

OF THE PREFERRED EMBODIMENTS

The following description is provided to enable any person skilled in the art to make and use the invention and sets forth the best modes contemplated by the inventors of carrying out their invention. Various modifications, however, will remain readily apparent to those skilled in the art, since the general principles of the present invention have been defined herein specifically to provide high speed, highly efficient CMOS imaging apparatus capable of increased resolution.

Figure 1 illustrates a conventional low voltage differential signaling (LVDS) circuit 11. The LVDS 11 circuit includes a current source I_1 (nominal 3.5mA) which drives one of the differential pair lines 13, 15. The receiver 17 has a high DC impedance (it does not source or sink DC current), so the majority of driver current flows across the 100 Ω termination resistor R_1 generating about 350mV across the receiver inputs 19, 21. When the driver 23 switches, it changes the direction of current flow across the resistor R_1, thereby creating a valid "one" or "zero" logic state.

comparison, an RS 422 driver typically delivers 3 volts across a 100 Ω termination, for 90 mW power consumption -- 75 times more than LVDS. Similarly, LVDS devices 11 require roughly one-tenth the power supply current of PECL/ECL devices.

Aside from the power dissipated in the load and static I_{CC} current, LVDS also lowers system power requirements through its CMOS current-mode driver design. This design greatly reduces the frequency component of I_{CC}. The I_{CC} vs. frequency plot for LVDS 11 is virtually flat between 10 MHz and 100 MHz for the quad devices (<50 mA total for driver + receiver at 100 MHz). In contrast, single ended, TTL/CMOS transceivers exhibit dynamic power consumption which increases exponentially with frequency.

To help ensure reliability, LVDS receivers 17 have a fail-safe feature that guarantees the output to be in a known logic state (HIGH) under certain fault conditions. These conditions include open, shorted, or terminated receiver inputs. If the driver 23 loses power, is disabled or is removed from the line, while the receiver 17 stays powered on with inputs terminated, the receiver output remains in a known state with the fail-safe feature.

If LVDS receivers 17 did not have the fail-safe feature and one of the fault conditions occurred, any external noise above the receiver thresholds could trigger the output and cause an error. A receiver without fail-safe could even go into oscillation under certain fault conditions. The fail-safe features ensures that the receiver output will be a HIGH -- rather than an unknown state -- under fault conditions.

Figure 2 illustrates CMOS video imaging sensing circuitry according to the preferred embodiment. This circuitry includes a CMOS image sensor chip 50 and an

Figure 2 illustrates CMOS video imaging sensing circuitry according to the preferred embodiment. This circuitry includes a CMOS image sensor chip 50 and an image processor chip 52. The CMOS image sensor chip 50 typically includes a number of light responsive CMOS pixel sensors which develop analog signals representative of an image. These analog signals are then A to D converted by the ADC circuit to form digital signals Din_0, Din_1 ... Din_n. The image processor chip 52 includes a data processor 53 which performs various manipulations of the image data such as compression and color processing. The processor 53 may be software driven or a hardware embodiment.

As may be seen, the circuit of Figure 2 employs a plurality of LVDS circuits 11. Each circuit 11 includes a respective driver 54 and a respective receiver 56. Each driver 54 receives a respective input signal Din_0, Din_1 ... Din_n, which are digital logic levels of, for example, 3.3 volts for logic "1" and zero volts for logic "0". Changes in state in these signals are transmitted over the differential lines to the respective receivers 56. Each receiver 56 generates a respective output signal $Dout_0$, $Dout_1$, ... $Dout_n$, which are at the several hundred milli-volt level.

In the preferred embodiment, the image sensor is a 1 Mega Pixel Sensor, and the pixel data is transferred at a rate of 30 MHz across the interface to the image processor 52, via 10 LVDS circuits 11. The circuitry of Figure 2 is preferably fabricated using CMOS fabrication technology, wherein the drivers 54 are formed as part of a silicon substrate-based CMOS image sensor chip 50 and the receivers 56 are formed as part of a silicon substrate-based signal processor chip 52. The leads or transmission lines 58, 60 then comprise metallic conductor paths laid out on a printed circuit board

between the two chips 50, 52. Various other embodiments could include an image sensor larger or smaller than 1 Mega Pixel, could operate at more or less than 30 MHz and could employ more or less than 10 LVDS circuits 11.

Those skilled in the art will appreciate that various adaptations and modifications of the just-described preferred embodiment can be configured without departing from the scope and spirit of the invention. Therefore, it is to be understood that, within the scope of the appended claims, the invention may be practiced other than as specifically described herein.

CLAIMS

What Is Claimed Is:

1. The CMOS imaging apparatus comprising:

a CMOS image sensor;

a CMOS image processor; and

a plurality of low voltage differential signaling circuits connected between said image sensor and said image processor.

2. The apparatus of Claim 1 wherein each of said plurality of low voltage differential signaling circuits comprises:

a CMOS driver circuit;

a CMOS receiver circuit; and

a pair of transmission lines interconnecting said driver circuit and said receiver circuit.

3. The apparatus of Claim 2 wherein said CMOS image sensor contains at least one million light responsive pixel image sensors.

4. The apparatus of Claim 3 wherein said plurality of low voltage differential signaling circuits comprise means for transferring data between said CMOS image sensor and said CMOS image processor at a data rate of 30 MHz or more.

5. The apparatus of Claim 4 wherein said plurality of low voltage differential signaling circuits comprises at least 10 low voltage differential signaling circuits.

6. The apparatus of Claim 5 wherein said CMOS image sensor and said CMOS driver circuits are formed on a first silicon circuit chip.

7. The apparatus of Claim 6 wherein said CMOS image processor circuit and said CMOS receiver circuits are formed on a second silicon circuit chip.

8. The apparatus of Claim 7 wherein each said pair of transmission lines resides on a surface located between said first and second circuit chips.

9. The apparatus of Claim 2 wherein each CMOS driver circuit receives a digital input signal from an analog to digital conversion circuit.

10. The apparatus of Claim 8 wherein each CMOS driver circuit receives a digital input signal from an analog to digital conversion circuit.

11. The CMOS imaging apparatus comprising:

a first silicon substrate chip having formed thereon a CMOS image sensor including an analog to digital converter circuit providing a plurality of digital pixel signal value output signals, said chip further including a CMOS driver circuit receiving as an input a selected one of said plurality of digital pixel signal value output signals and having first and second differential outputs.

12. The CMOS image apparatus of Claim 11 further including:

a second silicon substrate circuit chip having a CMOS digital signal processor formed thereon, said digital signal processor having a plurality of inputs connected to respective outputs of a plurality of CMOS receiver circuits, each CMOS receiver circuit having a pair of differential inputs adapted to be connected to said plurality of differential outputs.

13. The CMOS imaging apparatus of Claim 12 further including a pair of transmission lines connected between each respective pair of differential outputs and differential inputs.

14. The apparatus of Claim 12 wherein said CMOS image sensor contains at least one million light responsive pixel image sensors.

15. The apparatus of Claim 12 wherein said plurality of low voltage differential signaling circuits comprise means for transferring data between said CMOS image sensor and said CMOS image processor at a data rate of 30 MHz or more.

16. The apparatus of Claim 12 wherein said plurality of low voltage differential signaling circuits comprise at least 10 low voltage differential signaling circuits.

17. A method image processing comprising the step of:

developing an analog image signal using a plurality of CMOS image sensing pixels;

A-D converting said analog image signal to form a plurality of digital pixel value output signals; and

transferring said digital pixel value signals to a digital image processor through a plurality of low voltage differential signaling circuits.

18. The method of Claim 1 wherein a respective one of said low voltage differential circuits is selected to transfer a corresponding one of said digital signal pixel value signals.

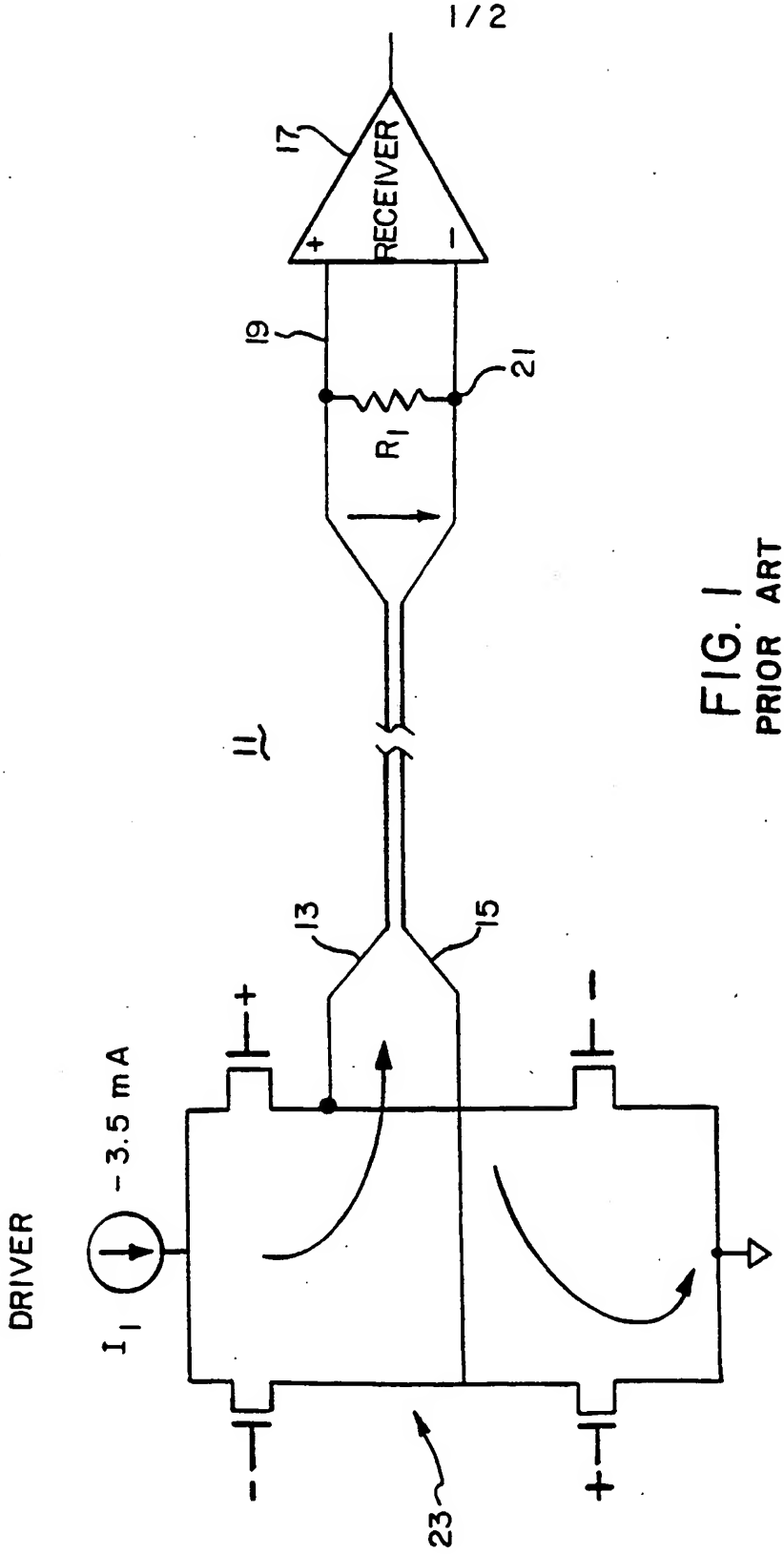
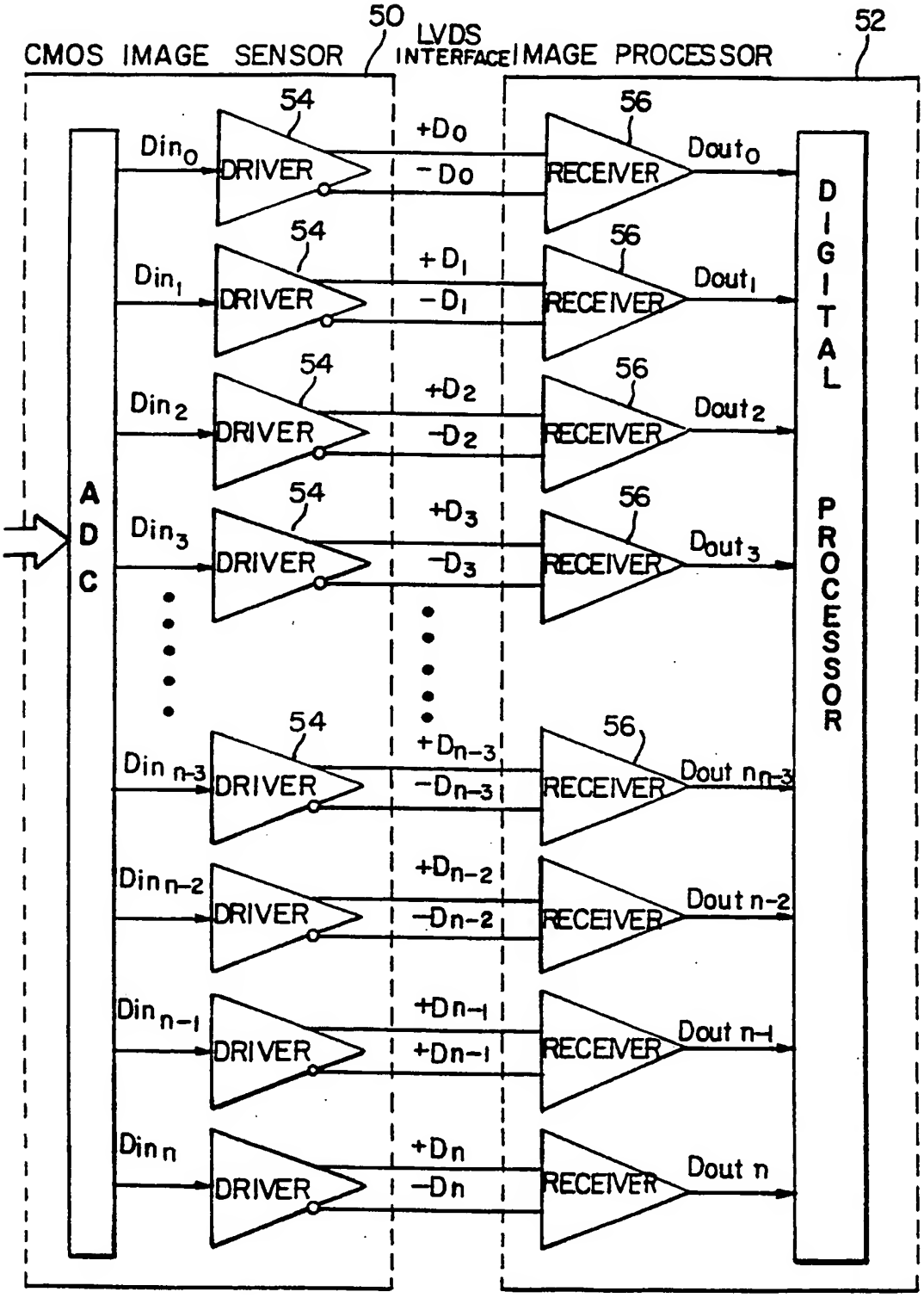


FIG. 1
PRIOR ART

FIG. 2


CMOS IMAGE SENSOR
50
LVDS INTERFACE
IMAGE PROCESSOR
52
ADC
DIGITAL PROCESSOR
Din0
Din1
Din2
Din3
Din n-3
Din n-2
Din n-1
Din n
DRIVER
54
+D0
-D0
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-D3
+Dn-3
-Dn-3
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Dout0
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Dout2
Dout3
Dout nn-3
Dout n-2
Dout n-1
Dout n

INTERNATIONAL SEARCH REPORT

Inter ..nal Application No
PCT/US 99/03262

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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INTERNATIONAL SEARCH REPORT

Information on patent family members

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